REMARKS/ARGUMENTS

In the Office Action dated May 4, 2007, claims 5 and 10 were rejected under 35 U.S.C. § 101 as lacking patentable utility. Claims 5 and 7-10 were rejected under 35 U.S.C. § 112, ¶2 as being indefinite. Claims 1-4, 6-9, 11, 12, 14, 16-18, 20, and 21 were rejected under 35 U.S.C. § 102(b) as being anticipated by Wakasugi, U.S. Patent No. 4,228,502 ("Wakasugi"). Claims 5, 10, 13, 15, and 19 were rejected under 35 U.S.C. § 103(a) as being obvious over Wakasugi.

Claims 1-16 and 21 are currently pending in this application. Claims 1-2, 4-7, 9, 11-13, 16, and 21 have been amended. Claims 17-20 have been canceled. No new matter has been added.

Regarding the rejections under 35 U.S.C. § 101 and 35 U.S.C. § 112, ¶2, claim 5 has been amended to overcome these rejections. Regarding claim 10, the rejections under 35 U.S.C. § 101 and 35 U.S.C. § 112, ¶2 are not understood. Claim 10 recites a first flip-flop for latching an output signal and a second flip-flop for latching an output. Therefore, the claim requires flip-flops that are capable of latching signals. Both S/R and D flip-flops are capable of the required latching and the precise circuitry required to implement either type of flip-flop is well-known to those of skill in the art. Therefore, the subject matter of claim 10 does have utility. Further, the phrase "the latch terminal" does not appear in claim 10. Therefore, this term cannot make claim 10 indefinite. Regarding the phrase "the control circuit sets", it is not understood what the Examiner means by the "dual meaning and function of the word sets." If the Examiner means that the word "sets" can be either a verb or a noun, it is clear from the context of the claims

that claims 7-10 use the word "sets" as a verb meaning to put into a particular state, rather than as a noun.

Regarding the rejections under 35 U.S.C. § 102(b), the Applicant respectfully submits that claims 1-4, 6-9, 11, 12, 14, 16, and 21 are not anticipated by Wakasugi. Wakasugi discloses an electronic computer system which automatically carries out initial program loading in response to an externally given signal such as a power-on signal, a system reset signal, etc., the initial program loading is not always carried out in response to the externally given signal but a higher priority request, if any, is first executed. Wakasugi teaches that, based on the position of mode switches, the program loading may be selected to occur automatically or to not occur automatically.

By contrast, the present invention is directed to controlling microcomputer circuits (such as those connected to pins of the microcomputer) that have multiple operations modes. Such operation modes include a given circuit being an input, an output, or an input/output, depending upon the mode that is set for the pin. The present invention is directed to preventing the operation mode of the pin from being changed in specified situations. In particular, claim 1 requires a protection circuit for protecting the input and output circuit from being reset in operation mode. The specified situation recited by claim 1 is from receiving a first signal of the write signal to receiving a reset signal from the outside once the control circuit has set the operation mode by receiving the first signal of the write signal.

Wakasugi does not disclose, suggest, or motivate preventing the operation mode of a circuit from being changed. Wakasugi further does not disclose, suggest, or motivate the specified situation recited by claim 1. Thus, Wakasugi does not teach, suggest, or

motivate a protection circuit in claim 1 for protecting the input and output circuit from being reset in operation mode from receiving a first signal of the write signal to receiving the reset signal from the outside once the control circuit has set the operation mode by receiving the first signal of write signal.

Claims 2, 6, 7, 9, and 11 require a control signal generator for generating a first output signal, being output during a first subsequence for a reset of the microcomputer and for generating a second output signal for setting an operation mode of an input and output circuit. Thus, claims 2, 6, 7, 9, and 11 require generating two output signals based on the recited conditions - during a first subsequence for a reset of the microcomputer and for setting an operation mode of an input and output circuit. Wakasugi does not teach, suggest, or motivate a control signal generator for generating a first output signal, which is output during a first subsequence for a reset of the microcomputer, and for generating a second output signal for setting an operation mode of an input and output circuit, as is required by claims 2, 6, 7, 9, 11. Wakasugi further does not teach, suggest, or motivate and a write protection circuit for generating a buffer signal in response to a first signal of the first output signal, as is required by claim 2. This requirement of claim 2 prevents a change in the operation mode of the circuit.

Wakasugi does not teach, suggest, or motivate a control circuit for latching a third output signal from the control signal generator in response to the write signal and for generating a control signal responsive to the a logical value of the third output signal latched in the control circuit, wherein the write signal is a signal with a fixed logical value if the logical value of the second output signal latched in the write protection circuit is "0", the write signal is a buffer signal that is the buffered version of the first output

signal from the control signal generator if a logical value of the second output signal latched in the write protection circuit is "1", and the control signal is supplied to a selection circuit that selects one signal generator from among a plurality of signal generators, each containing at least a data register, for sending a signal to the outside, as required by claim 12.

Wakasugi does not teach, suggest, or motivate the write signal that is a signal with a fixed logical value if a logical value of the second output signal latched in the write protection circuit is "0", the write signal being a buffer signal that is a buffered version of the first output signal if a logical value of the second output signal latched in the write protection circuit is "1", as required by claim 16.

Wakasugi does not teach, suggest, or motivate a watchdog timer wherein the watchdog timer outputs the first reset signal to the microcomputer when the monitoring signal is interrupted, as required by claim 21.

Therefore, claims 1, 2, 6, 7, 9, 11, 12, 16, and 21, and claims 3-4, 8, and 14, which depend therefrom, are not anticipated by Wakasugi.

The Applicant respectfully submits that claims 5 and 7-10 are not obvious over Wakasugi, because even if Wakasugi were modified as suggested by the Examiner, the result still would not disclose or suggest the requirements of the claims.

As discussed above, Wakasugi does not teach, suggest, or motivate certain requirements of claims 2, 7, and 9, from which claims 5, 8, and 10 depend. Even if Wakasugi were modified as suggested by the Examiner, the suggested modification still would not cure the deficiencies of these claims with respect to these required elements.

In addition, Wakasugi does not teach, suggest, or motivate a flip-flop with a reset terminal and a clock terminal thereof connected to an output terminal of the AND gate, for outputting a signal having a logical signal "0" when the reset signal is received at the reset terminal and for outputting a signal having a logical signal "1" when a pulse signal is received at the clock terminal thereof, as required by claim 5.

Wakasugi does not teach, suggest, or motivate a first control circuit wherein the write signal responsive to the logical value of the second output signal from the control signal generator is a signal with a fixed logical value if a logical value of the second output signal latched in the write protection circuit is "0", the write signal is a buffer signal that is a buffered version of the first output signal from the control signal generator if a logical value of the ' second output signal latched in the write protection circuit is "1", as required by claim 13.

Therefore, claims 5 and 7-10 are not obvious over Wakasugi as modified by the Examiner.

Each of the claims now pending in this application is believed to be in condition for allowance. Accordingly, favorable reconsideration of this case and early issuance of the Notice of Allowance are respectfully requested.

Additional Fees:

The Commissioner is hereby authorized to charge any insufficient fees or credit any overpayment associated with this application to Deposit Account No. 50-4047 (4195460067).

Conclusion

In view of the foregoing, all of the Examiner's rejections to the claims are believed to be overcome. The Applicants respectfully request reconsideration and issuance of a Notice of Allowance for all the claims remaining in the application. Should the Examiner feel further communication would facilitate prosecution, he is urged to call the undersigned at the phone number provided below.

Respectfully Submitted,

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